

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	2	((("6757347") or ("6912679")).PN.	USPAT; USOCR	OR	OFF	2005/11/08 15:53
S2	615	(703/14).CCLS.	USPAT; USOCR	OR	OFF	2005/11/08 15:54
S3	2	S2 and metastab\$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/08 16:00
S4	5	simulat\$5 same synthesis same metastab\$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/08 16:03
S5	284	simulat\$5 and synthesis and metastab\$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/08 16:03
S6	64	simulat\$5 and synthesis and metastab\$4 and (flip flop\$2)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/08 16:22
S7	3	simulat\$5 and synthesis and metastab\$4 and (plurality adj3 (flip flop\$2))	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/08 16:04
S8	9	S6 and @py<="2001"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/08 16:15
S9	1	("6198324").PN.	USPAT; USOCR	OR	OFF	2005/11/08 16:22
S10	35	simulat\$4 and metastable and verilog	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/15 12:47
S11	0	simulat\$4 and metastable and flip-flop\$s2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/15 12:47
S12	199	simulat\$4 and metastable and flip-flop\$2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/15 12:52

S13	143	simulat\$4 and metastable and flip-flop\$2 and random	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/15 12:48
S14	32	simulat\$4 and metastable and flip-flop\$2 and random adj number\$2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/15 12:48
S15	145	simulat\$4 and metastable and flip-flop\$2 and generator	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/15 12:52
S16	117	simulat\$4 and metastable and flip-flop\$2 and generator and random	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/15 12:52
S17	111	simulat\$4 and metastable and flip-flop\$2 and generator and random and bus	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/15 12:52
S18	99	simulat\$4 and metastable and flip-flop\$2 and generator and random and bus and processor	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/15 12:53
S19	19	simulat\$4 and metastable and flip-flop\$2 and generator and random and bus and processor and synthes\$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/15 12:56
S20	4337	random near number\$2 and simulation	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/15 12:56
S21	89	random near number\$2 and simulation and metast\$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/15 12:57
S22	39	random near number\$2 and simulation and metast\$4 and flip	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/15 12:57
S23	618	(703/14).CCLS.	USPAT; USOCR	OR	OFF	2005/11/15 13:02

S24	123	S23 and flip	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/15 14:37
S25	1	S23 and flip and metastable	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/15 13:05
S26	11	("4907180"   "5051941"   "5278769"   "5297066"   "5305229"   "5553008"   "5701254"   "5703798"   "5822567"   "6190433"   "6311146").PN. OR ("6408264").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2005/11/15 13:06
S27	1	("6408265").PN.	USPAT; USOCR	OR	OFF	2005/11/15 14:44
S28	49	simulat\$5 and metastab\$4 and rank\$3 and boundary	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/15 14:45
S29	45	simulat\$5 and metastab\$4 and rank\$3 and boundary and random	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/15 14:45
S30	28	simulat\$5 and metastab\$4 and rank\$3 and boundary and random adj number\$2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/15 14:47
S31	4	simulat\$5 same metastab\$4 and rank\$3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/15 14:47
S32	23	simulat\$5 same metastab\$4 and random	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/15 14:47
S33	8	("4982118"   "5014226"   "5517658"   "5539652"   "5544067"   "5826061"   "5850355").PN. OR ("6408265").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2005/11/15 14:54
S34	0	("W927472.PTPN.").PN.	USPAT; USOCR	OR	OFF	2005/11/15 14:57
S35	0	("20010124.FRPD.").PN.	USPAT; USOCR	OR	OFF	2005/11/15 14:58
S36	0	"20010124".FRPD.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/11/15 14:58

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Verilog and metastable and (random number)

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lections of PLAs and **Random** logic. hexadecimal **numbers** in base 16. high-level programming language A por- ... flip-flop enters A **metastable** state and where ...

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Compute A **random** integral nonlinearity. **number** random\_inl = (2\*rand()-1)\*inl ... in A **metastable** state (A conversion error occurs) ...

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**number** of **random** patterns to simulate. The larger that ... **Verilog** is a registered trademark of Cadence Design Systems,. Inc. References ...

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of **Verilog numbers** 486. Base Connectivity Model (BCM), in CFI. standard 372 ... **metastable** hardened 253. setup time 73. slave latch 71. synchronizer 253 ...

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input **numbers** have higher priorities). 5.2.3 Generated **Verilog** ... a latch remaining in a **metastable** state (ie not resolving to a valid logic-1 or ...

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synthesis from **Verilog** is an alternative to the. typical implementation of such a ... The **number** of bits. representing the tens of minutes and tens of ...

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... Monte-Carlo simulation and using different kinds of **random number** generators. ... The influence of the doping and hydrogen content on **metastable** ...

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quenched forming defects or freezing out in **metastable** states (ie. trapped in a local ... a **random number** between 0 and 1 is generated, and if it falls ...



verilog and metastable

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### Synthesis and Scripting Techniques for Designing Multi-Asynchronous Clock Designs

CE Cummings - Synopsys Users Group Conference, San Jose, CA, www. sunburst ..., 2001 - vlsidsp.el.yuntech.edu.tw

... adat bdat1 ack bclk Clocked signal is initially **metastable** ... .. and might still be **metastable** at the next rising edge of bclk ack is asynchronous to bclk ...

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### SAME 2004

S Bernardi, S Lebailly, T Instruments, B Blanc, G ... - signal - same-conference.org

... If the first flip-flop enters the **metastable** condition, it has a full clock ... have been compared to the one obtained by the hand-written **Verilog** design, under ...

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### Synchronous Resets? Asynchronous Resets? I am so confused! How will I ever know which to use?

CE Cummings, D Mills - SNUG 2002 (Synopsys Users Group Conference, San Jose, CA, ..., 2002 - sunburst-design.com

... of the reset so as to prevent the chip from going into a **metastable** unknown state ...

The **Verilog**-2001 Standard[17] has three built-in commands to model and test ...

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### Asynchronous & Synchronous Reset Design Techniques-Part Deux

CE Cummings, D Mills, S Golson - SNUG Boston 2003 - sunburst-design.com

... of the reset so as to prevent the chip from going into a **metastable** unknown state ...

The **Verilog**-2001 Standard[29] has three built-in commands to model and test ...

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### The Design and Implementation of a Fast, Low-power, Asynchronous Router Chip

CR Jesshope, P North, N Zealand, I Swarbrick - www-ist.massey.ac.nz

... Circuit schematics, silicon layouts and **Verilog** models were created for each of the cells. ... circuit, there is a (small) possibility that a **metastable** state will ...

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### 10-3

DRL LSI-PCA - ieeexplore.ieee.org

... the element suppresses **metastable** outputs until it gets out of a **metastable** condition even ... designed by describing their net-lists directly with HDL (**Verilog** HDL ...

[Web Search](#)

### Asynchronous communication mechanisms using self-timed circuits

F Xia, A Yakovlev, D Shang, A Bystrov, A Koelmans, ... - Proc. Async2000, Eilat, Israel, 2000 - doi.ieeecomputersociety.org

... these ACMS is shown in Figure 2. Fundamental mode assumptions on control variable operations do not hold when such shared variables become **metastable**, which is ...

Cited by 16 - [Web Search](#) - [ieeexplore.ieee.org](#) - [doi.ieeeecs.org](#) - [staff.ncl.ac.uk](#) - [all 7 versions](#) »

### Channel Communication Between Independent Clock Domains

S Moore, G Taylor, B Mullins, P Robinson - First ACiD-WG Workshop of the European Commission's Fifth ..., 2001 - [scism.sbu.ac.uk](http://scism.sbu.ac.uk)

... and req changes around the same time then the arbiter may go **metastable**. ... Simulations were performed using **Verilog** with SDF annotation using the the VST/UMC ...

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### Point to point GALS interconnect

S Moore, G Taylor, R Mullins, P Robinson - Proceedings of the Eighth International Symposium on Advanced ..., 2002 - [ieeexplore.ieee.org](http://ieeexplore.ieee.org)

... and req changes around the same time then the arbiter may go **metastable**. ... Simulations were performed using **Verilog** with SDF annotation using the VST/UMC 0.25 m ...

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### A reliability testing environment for off-the-shelf memory subsystems

SH Hwang, GS Choi - IEEE Design and Test of Computers, 2000 - [ieeexplore.ieee.org](http://ieeexplore.ieee.org)

... of sup- porting logic—memory controller, for example—written in **Verilog** HDL form ... With 0.02-picocoulomb (pC) injection, a **metastable** state occurs around the ...

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